REMARKS

The Office Action dated October 1, 2003 has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto. Currently, claims 2-10 have been allowed and claims 11-35 have been withdrawn from consideration. By this Amendment, claim 1 has been amended to more particularly point out and distinctly claim the invention, and claims 47 and 48 have been newly added. No new matter has been added or amendments made that narrow the scope of any elements of any claims. Accordingly, claims 1-48 are pending in this application. Claims 1, 36-43, 47 and 48 are submitted for consideration.

Applicants acknowledge and thank the Examiner for indicating that claims 2-10 are allowed over the prior art.

Claims 1 and 36-43 were rejected under 35 U.S.C. § 102(e) as being anticipated by Okutsu et al. (U.S. Patent No. 6,433,623, "Okutsu"). However, Applicants respectfully submit that claims 1 and 36-43 recite subject matter that is neither disclosed nor suggested in Okutsu.

Applicants' amended claim 1 recites a level shift circuit including a capacitor and a charge control circuit connected to the capacitor for providing a voltage of a high potential power supply to the capacitor and controlling charging of the capacitor. A limiting circuit is connected to the high potential power supply and the charge control circuit for stopping the voltage provided to the capacitor from the high potential power supply before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor.

Applicants' claim 36 recites a level shift circuit including a capacitor and a first transistor connected to the capacitor for providing a voltage of a high potential power supply to the capacitor and controlling charging of the capacitor. A second transistor is connected to the high potential power supply and the first transistor for being turned off before the first transistor is turned off when boosting of an output signal of the level shift circuit to a boosted voltage, which is higher than the voltage of the high potential power supply, is started.

Applicants' claim 43 recites a level shift circuit including a capacitor and a charge control circuit connected to the capacitor, for providing a voltage of a high potential power supply to the capacitor and controlling charging of the capacitor. A limiting circuit is connected to the high potential power supply and the charge control circuit, for limiting the voltage provided to the capacitor from the high potential power supply before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor. The limiting circuit limits the voltage provided to the capacitor when charging of the capacitor to a boosted voltage, which is higher than the voltage of the high potential power supply, is started.

In making this rejection, the Office Action took the position that Okutsu discloses all of the elements of the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest the structure of the claimed invention, and therefore, fails to provide the advantages of the present invention. For example, the shift level circuit of the present invention includes a capacitor and a charge control circuit connected to the capacitor that provides a voltage of a high potential power supply to the capacitor and also controls the capacitor. A limiting circuit is connected to

the high potential power supply and the charge control circuit for stopping the voltage provided to the capacitor from the high potential power supply, before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor.

As a result of this claimed configuration, when the capacitor performs voltage step-up, the current limiting circuit limits the charge that leaks from the capacitor to the high potential power supply and increases the voltage step-up efficiency. This improves the response of the output signal in the level shift circuit.

The present invention is characterized by the limiting circuit stopping the voltage provided to the capacitor from the high potential power supply before the charge control circuit in order to overcome the conventional problem that causes a current leak and lowers an operational speed of the level shift circuit even if a charge control circuit stops supplying a high potential power supply voltage to a capacitor when a level shift of the capacitor is initiated.

Okutsu discloses that the PMOS transistor (P12) of a charge control circuit and the PMOS transistor (P13) of a limiting circuit are simultaneously turned off. In contrast, the limiting circuit, for example, (21; 21A; Q2) of the present invention stops supplying the voltage of the high potential power supply to the capacitor before the charge control circuit (Q1), as recited in claims 1 and 43.

Furthermore, Applicants' claim 36 further recites that the level shift circuit includes a second transistor connected to the high potential power supply and the first transistor, which is turned off before the first transistor is turned off when boosting of an output signal of a level shift circuit to a boosted voltage is started.

However, Okutsu fails to suggest this limitation. As discussed above, in Okutsu, the first transistor (PMOS transistor P12) and second transistor (the PMOS transistor P13) are simultaneously turned off.

Therefore, it is respectfully submitted that the Applicants' invention, as set forth in claims 1 and 36-43, is not anticipated within the meaning of 35 U.S.C. § 102.

Newly added claim 47 is dependent upon claim 1 and further recites a level shift circuit, wherein the charge control circuit includes an inverter provided between the high potential power supply and a low potential power supply.

Newly added claim 48 recites a level shift circuit including a capacitor and a charge control circuit connected to the capacitor for providing a voltage of a high potential power supply to the capacitor in accordance with a first control signal and controlling charging of the capacitor. A limiting circuit is connected to the high potential power supply and the charge control circuit for stopping the voltage provided to the capacitor from the high potential power supply in accordance with a second control signal that changes faster, based on an input signal, than the first control signal.

Therefore, it is respectfully submitted that newly added claims 47 and 48 are patentable over the applied references.

Still further, As claims 37-39 depend from claim 36, and claims 40-42 and 47 depend from claim 1, Applicants submit that each of these claims recite subject matter that is neither disclosed nor suggested by the cited prior art for at least the reasons set forth above with respect to the independent claim.

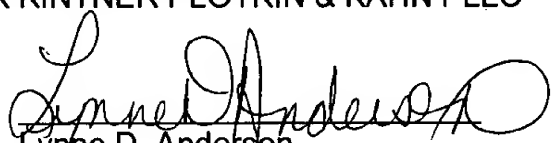
In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1, 36-43, 47 and 48 (claims 2-10 already

being allowed), and the prompt issuance of a Notice of Allowability are respectfully solicited.

If this application is not in condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108075-00054.**

Respectfully submitted,
ARENT FOX KINTNER PLOTKIN & KAHN PLLC



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